METHOD FOR PROVIDING REMOTE SOFTWARE TECHNOLOGICAL SUPPORT

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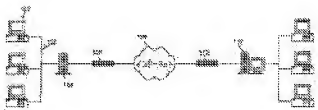
Publication date: 1998-08-21
Inventor(s): TIMOTHY J SOUTHGATE
Applicant(s): ALTERA CORP
Classification:
- international: ***G01R31/317; G01R31/3177; G01R31/3185; G06F9/445; G06F11/14; G06F11/28; G06F12/00; G06F17/50; H01L21/82;* G06F12/00; G01R31/28; G06F9/445; G06F11/14; G06F11/28; G06F17/50; H01L21/70;** (IPC1-7): G06F9/445
- European: G01R31/3177; G01R31/3185P; G06F9/445N; G06F11/14A4B; G06F17/50; G06F17/50C3E; G06F17/50D; G06F17/50D4
Application number: JP19970294544 19971027
Priority number(s): US19960029277P 19961028

Also published as:
GB2321322 (A)
JP10232891 (A)
JP10232890 (A)
GB2318665 (A)
GB2318664 (A)

Abstract of **JP 10222374 (A)**

PROBLEM TO BE SOLVED: To update customer's software remotely by overwriting software by updating from a vendor when the customer and vendor has different data on versions regarding the software. SOLUTION: Each time a user starts executing software, an Internet-106 connection with a vendor is established. Then known bug data are downloaded to a user platform 100 from a vendor platform 110 together with version data on respective software modules. At this time, when it becomes evident from a comparison result that modules of the user's software is old, a dialog box inquiring whether or not the user desires to update those modules is displayed to the user. Here, when the user desires, modules of the latest version in an upgrade list are downloaded from the vendor and overwritten to the corresponding old modules on the user platform 100.



Family list
Approximately **33** application(s) for: JP10222374 (A)

1 **Embedded logic analyzer**

Inventor: VEENSTRA KERRY [US] ; RANGASAYEE KRISHNA [US] (+1)
EC: G06F11/27; G01R31/3177
Applicant: ALTERA CORP [US]
IPC: ***G06F11/22; G06F11/25; G01R31/28;*** (+15)
Publication info: **DE69834892 (T2)** — 2007-05-24

2 **Embedded logic analyzer**

Inventor: VEENSTRA KERRY [US] ; RANGASAYEE KRISHNA [US] (+1)
EC: G06F11/27; G01R31/3177
Applicant: ALTERA CORP [US]
IPC: ***G06F11/22; G06F11/25; G01R31/28;*** (+15)
Publication info: **DE69835106 (T2)** — 2006-12-07

3 **Embedded logic analyzer**

Inventor: VEENSTRA KERRY [US] ; RANGASAYEE KRISHNA [US] (+1)
EC: G06F11/27; G01R31/3177
Applicant: ALTERA CORP [US]
IPC: ***G06F11/22; G01R31/28; G01R31/3177;*** (+14)
Publication info: **EP0919916 (A2)** — 1999-06-02
EP0919916 (A3) — 2000-01-12
EP0919916 (B1) — 2006-06-14

4 **Embedded logic analyser**

Inventor: VEENSTRA KERRY [US] ; RANGASAYEE KRISHNA [US] (+1)
EC: G01R31/3177; G06F11/27; (+1)
Applicant: ALTERA CORP [US]
IPC: ***G01R31/3177; G06F11/27; G06F11/36;*** (+6)
Publication info: **EP1233341 (A1)** — 2002-08-21
EP1233341 (B1) — 2006-06-28

5 **Enhanced embedded logic analyzer**

Inventor: VEENSTRA KERRY [US] ; RANGASAYEE KRISHNA [US] (+1)
EC: G01R31/3177; G06F11/27; (+1)
Applicant: ALTERA CORP [US]
IPC: ***G06F11/27; G01R31/317; G01R31/3177;*** (+4)
Publication info: **EP1677195 (A2)** — 2006-07-05

6 **Work group computing for electronic design automation**

Inventor: FAIRBANKS BRENT ALAN [US] ; HEILE FRANCIS BERNARD [US]
EC: G01R31/3185P; G06F9/44G4C; (+4)
Applicant: ALTERA CORP [US]
IPC: ***G01R31/3185; G06F9/44; G06F11/14;*** (+6)
Publication info: **GB2346242 (A)** — 2000-08-02
GB2346242 (B) — 2000-09-27

7 **Embedded logic analyzer for a programmable logic device**

Inventor: HERRMAN ALAN LOUIS ; NUGENT GREG PATRICK
EC: G01R31/3177; G01R31/3185P; (+6)
Applicant: ALTERA CORP [US]
IPC: ***G01R31/317; G01R31/3177; G01R31/3185;*** (+15)
Publication info: **GB2318664 (A)** — 1998-04-29
GB2318664 (B) — 2000-08-23

8 **Work group computing for electronic design automation**

Inventor: FAIRBANKS BRENT ALAN ; HEILE FRANCIS BERNARD
EC: G01R31/3177; G01R31/3185P; (+6)
Applicant: ALTERA CORP [US]
IPC: ***G01R31/317; G01R31/3177; G01R31/3185;*** (+14)

Publication info: **GB2318665 (A)** — 1998-04-29
GB2318665 (B) — 2000-06-28

9 **Remote technical support for software**

Inventor: SOUTHGATE TIMOTHY JAMES **Applicant:** ALTERA CORP [US]
EC: G01R31/3177; G01R31/3185P; (+6) **IPC:** ***G01R31/317; G01R31/3177; G01R31/3185;*** (+14)
Publication info: **GB2321322 (A)** — 1998-07-22
GB2321322 (B) — 2001-10-10

10 **METHOD FOR PROVIDING REMOTE SOFTWARE TECHNOLOGICAL SUPPORT**

Inventor: TIMOTHY J SOUTHGATE **Applicant:** ALTERA CORP
EC: G01R31/3177; G01R31/3185P; (+6) **IPC:** ***G01R31/317; G01R31/3177; G01R31/3185;*** (+14)
Publication info: **JP10222374 (A)** — 1998-08-21

11 **INTEGRATED LOGIC ANALYZER FOR PROGRAMMABLE LOGIC CIRCUIT**

Inventor: ALAN L HERMANN ; GREGG P NUJENT **Applicant:** ALTERA CORP
EC: G01R31/3177; G01R31/3185P; (+6) **IPC:** ***G01R31/317; G01R31/3177; G01R31/3185;*** (+16)
Publication info: **JP10232890 (A)** — 1998-09-02

12 **WORK GROUP COMPUTING FOR ELECTRONIC DESIGN AUTOMATION**

Inventor: HEILE FRANCIS B ; FAIRBANKS BRENT A **Applicant:** ALTERA CORP
EC: G01R31/3177; G01R31/3185P; (+6) **IPC:** ***G01R31/317; G01R31/3177; G01R31/3185;*** (+16)
Publication info: **JP10232891 (A)** — 1998-09-02

13 **IMPROVED EMBEDDED LOGIC ANALYZER**

Inventor: VEENSTRA KERRY ; RANGASAYEE KRISHNA (+1) **Applicant:** ALTERA CORP
EC: G06F11/27; G01R31/3177 **IPC:** ***G06F11/22; G01R31/28; G01R31/3177;*** (+18)
Publication info: **JP11296403 (A)** — 1999-10-29

14 **Work group computing for electronic design automation**

Inventor: HEILE FRANCIS B [US] ; FAIRBANKS BRENT A [US] **Applicant:** ALTERA CORP [US]
EC: G01R31/3177; G01R31/3185P; (+7) **IPC:** ***G01R31/3177; G01R31/3185; G06F9/44;*** (+9)
Publication info: **US5983277 (A)** — 1999-11-09

15 **Local compilation in context within a design hierarchy**

Inventor: HEILE FRANCIS B [US] ; RAWLS TAMLYN V [US] (+3) **Applicant:** ALTERA CORP [US]
EC: G01R31/3185P; G06F9/44G4C; (+5) **IPC:** ***G01R31/3185; G06F9/44; G06F9/445;*** (+8)
Publication info: **US6026226 (A)** — 2000-02-15

Family list
Approximately **33** application(s) for: JP10222374 (A)

16 **Fitting for incremental compilation of electronic designs**
Inventor: TSE JOHN [US] ; LEE FUNG FUNG [US] (+1) **Applicant:** ALTERA CORP [US]
EC: G06F17/50D4; G06F9/44G4C; (+2) **IPC:** ***G06F9/44; G06F9/445; G06F17/50;*** (+4)
Publication info: **US6102964 (A)** — 2000-08-15

17 **Graphic editor for block diagram level design of circuits**
Inventor: SOUTHGATE TIMOTHY J [US] ; WENZLER MICHAEL [US] **Applicant:** ALTERA CORP [US]
EC: G06Q10/00F; G01R31/3177; (+6) **IPC:** ***G01R31/3177; G01R31/3185; G06F9/44;*** (+9)
Publication info: **US6110223 (A)** — 2000-08-29

18 **Design file templates for implementation of logic designs**
Inventor: SOUTHGATE TIMOTHY J [US] ; WENZLER MICHAEL [US] **Applicant:** ALTERA CORP [US]
EC: G06F9/44G4C; G06F9/445N; (+2) **IPC:** ***G06F9/44; G06F9/445; G06F17/50;*** (+4)
Publication info: **US6120550 (A)** — 2000-09-19

19 **Generation of sub-netlists for use in incremental compilation**
Inventor: PEDERSEN BRUCE [US] ; HEILE FRANCIS B [US] (+2) **Applicant:** ALTERA CORP [US]
EC: G01R31/3177; G01R31/3185P; (+8) **IPC:** ***G01R31/3177; G01R31/3185; G06F9/44;*** (+11)
Publication info: **US6134705 (A)** — 2000-10-17

20 **Method and apparatus for automated circuit design**
Inventor: SOUTHGATE TIMOTHY J [US] **Applicant:** ALTERA CORP [US]
EC: G06F9/44G4C; G06F17/50C3E; (+1) **IPC:** ***G06F9/44; G06F17/50;*** **G06F9/44;** (+2)
Publication info: **US6161211 (A)** — 2000-12-12

21 **Embedded logic analyzer for a programmable logic device**
Inventor: HERRMANN ALAN L [US] ; NUGENT GREG P [US] **Applicant:** ALTERA CORP [US]
EC: G01R31/3177; G01R31/3185P; (+8) **IPC:** ***G01R31/3177; G01R31/3185; G06F9/44;*** (+12)
Publication info: **US6182247 (B1)** — 2001-01-30

22 **Method for providing remote software technical support**
Inventor: SOUTHGATE TIMOTHY J [US] **Applicant:** ALTERA CORP [US]
EC: G06F9/44G4C; G06F9/445N; (+2) **IPC:** ***G06F9/44; G06F9/445; G06F11/273;*** (+6)
Publication info: **US6205579 (B1)** — 2001-03-20

23 **Enhanced embedded logic analyzer**
Inventor: BEENSTRA KERRY [US] ; RANGASAYEE KRISHNA [US] (+1) **Applicant:** ALTERA CORP [US]
EC: G01R31/3177; G01R31/3185P; (+1) **IPC:** ***G01R31/3177; G01R31/3185; G06F17/50;*** (+3)
Publication info: **US6247147 (B1)** — 2001-06-12

24 **Enhanced embedded logic analyzer**
Inventor: VEENSTRA KERRY [US] ; **Applicant:** ALTERA CORP [US]

RANGASAYEE KRISHNA [US] (+1)
EC: G06F17/50C3E; G01R31/3177; (+2) **IPC:** ***G01R31/3177; G01R31/3185; G06F11/27;*** (+7)
Publication info: **US6286114 (B1)** — 2001-09-04

25 **Incremental compilation of electronic design for work group**

Inventor: HEILE FRANCIS B [US] ; FAIRBANKS BRENT A [US] **Applicant:** ALTERA CORP [US]
EC: G01R31/3177; G01R31/3185P; (+7) **IPC:** ***G01R31/3177; G01R31/3185; G06F9/44;*** (+9)
Publication info: **US6298319 (B1)** — 2001-10-02

26 **Methods and apparatus for simulating a portion of a circuit design**

Inventor: SOUTHGATE TIMOTHY J [US] **Applicant:** ALTERA CORP [US]
EC: G06F9/445N; G06F17/50C3; (+1) **IPC:** ***G06F9/445; G06F17/50;*** **G06F9/445;** (+2)
Publication info: **US6311309 (B1)** — 2001-10-30

27 **Electronic design automation tool for display of design profile**

Inventor: HEILE FRANCIS B [US] **Applicant:** ALTERA CORP [US]
EC: G06F17/50D; G06F17/50D4 **IPC:** ***G06F17/50;*** **G06F17/50;** (IPC1-7): G06F17/50
Publication info: **US6317860 (B1)** — 2001-11-13

28 **Interface for compiling project variations in electronic design environments**

Inventor: HEILE FRANCIS B [US] ; RAWLS TAMLYN V [US] **Applicant:** ALTERA CORP [US]
EC: G06Q10/00C; G06F17/50D **IPC:** ***G06F9/44; G06F9/445; G06F17/50;*** (+6)
Publication info: **US6321369 (B1)** — 2001-11-20

29 **Embedded logic analyzer for a programmable logic device**

Inventor: HERRMANN ALAN L [US] ; NUGENT GREG P [US] **Applicant:** ALTERA CORP [US]
EC: G01R31/3177; G01R31/3185P; (+8) **IPC:** ***G01R31/3177; G01R31/3185; G06F9/44;*** (+12)
Publication info: **US6389558 (B1)** — 2002-05-14

30 **Enhanced embedded logic analyzer**

Inventor: VEENSTRA KERRY [US] ; RANGASAYEE KRISHNA [US] (+1) **Applicant:** VEENSTRA KERRY, ; RANGASAYEE KRISHNA, (+2)
EC: G01R31/3177; G01R31/3185P; (+3) **IPC:** ***G01R31/3177; G01R31/3185; G06F11/27;*** (+7)
Publication info: **US2001037477 (A1)** — 2001-11-01
US6460148 (B2) — 2002-10-01

Family list
33 application(s) for: **JP10222374 (A)**

31 **Generation of sub-netlists for use in incremental compilation**

Inventor: PEDERSEN BRUCE [US] ; HEILE FRANCIS B [US] (+2)
Applicant: ALTERA CORP [US]
EC: G01R31/3177; G01R31/3185P; (+8)
IPC: ***G01R31/3177; G01R31/3185; G06F9/44;*** (+11)
Publication info: **US6490717 (B1)** — 2002-12-03

32 **Graphic editor for block diagram level design of circuits**

Inventor: SOUTHGATE TIMOTHY J [US] ; WENZLER MICHAEL [US]
Applicant: ALTERA CORP [US]
EC: G06Q10/00F; G01R31/3177; (+6)
IPC: ***G01R31/3177; G01R31/3185; G06F9/44;*** (+9)
Publication info: **US6588004 (B1)** — 2003-07-01

33 **Enhanced embedded logic analyzer**

Inventor: VEENSTRA KERRY [US] ; RANGASAYEE KRISHNA [US] (+1)
Applicant: ALTERA CORP A DELAWARE CORP [US]
EC: G01R31/3177; G01R31/3185P; (+3)
IPC: ***G01R31/3177; G01R31/3185; G06F11/27;*** (+7)
Publication info: **US2002194543 (A1)** — 2002-12-19
US6704889 (B2) — 2004-03-09

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